AMENDMENTS TO THE CLAIMS

Claims 1-36 (Cancelled)

37. (New) A memory model comprising:

a memory primitive;

a read data port primitive for coupling to an output port of the memory primitive;

an address bus primitive for coupling to the memory primitive and the read data port primitive;

a data bus primitive for coupling to the memory primitive; and

a plurality of memory out primitives, each memory out primitive for coupling to the read data port primitive.

38. (New) The memory model of Claim 37, wherein the memory primitive includes:

a set input port;

a reset port;

a write_clock port;

a write_enable port;

a write_address port for coupling to an output of the address bus primitive;

a write_data port for coupling to an output of the data bus primitive; and

an output port for coupling to an input of the read data port primitive.

39. (New) The memory model of Claim 37, wherein the read data port primitive represents a read port functionality of the memory.

40. (New) The memory model of Claim 39, wherein the read data port primitive includes:

a read enable port;

a read_address port for coupling to the address bus primitive;

a read_data port for coupling to the memory primitive; and

an output port for coupling to the plurality of memory out primitives, wherein a dimension of the output port corresponds to a data dimension of the memory primitive.

41. (New) The memory model of Claim 37, wherein the address bus primitive represents an address functionality of a memory.

42. (New) The memory model of Claim 41, wherein the address bus primitive includes:

a plurality of input ports corresponding to an address dimension of the memory primitive; and

an output port for coupling to the memory primitive and the read data port primitive.

43. (New) The memory model of Claim 42, wherein the address bus primitive further includes an attribute indicating whether an incoming address is encoded or decoded.

44. (New) The memory model of Claim 43, wherein the data bus primitive represents a data bus functionality of the memory.

45. (New) The memory model of Claim 44, wherein the data bus includes:

a plurality of input ports corresponding to a data dimension of the memory primitive; and

an output port for coupling to the memory primitive.

46. (New) The memory model of Claim 37, wherein each memory out primitive represents a simulated value storage functionality of the memory.

47. (New) The memory model of Claim 46, wherein each memory out primitive includes:

an input port; and

an output port.

48. (New) The memory model of Claim 37, wherein a plurality of tristate drivers can be coupled to output ports of the memory out primitives, thereby representing an attribute of the read data port primitive.

49. (New) The memory model of Claim 37, wherein a plurality of edge-triggered registers can be coupled to output ports of the memory out primitives, thereby representing an attribute of the read data port primitive.

50. (New) The memory model of Claim 49, wherein a plurality of tristate drivers can be coupled to output ports of the plurality of edge-triggered registers, thereby representing an attribute of the read data port primitive.

51. (New) A content addressable memory model comprising:

a memory primitive;

a compare port primitive for coupling to an output port of the memory primitive;

an address bus primitive for coupling to the memory primitive and the compare port primitive;

a data bus primitive for coupling to the memory primitive; and

a plurality of memory output primitives, each memory output primitive for coupling to the compare port primitive.

52. (New) The memory model of Claim 51, wherein the compare port primitive includes:

a compare enable port;

a data bus port for coupling to an output port of the data bus primitive;

a data port for coupling to an output port of the memory primitive; and

an output port for coupling to input ports of the plurality of memory output primitives.

53. (New) A combined content addressable memory (CAM) and random access memory (RAM) model comprising:

a first memory primitive;

a data bus primitive;

a compare port primitive for coupling to the memory primitive and the data bus primitive;

a plurality of memory output primitives, each memory output primitive for coupling to the compare port primitive;

an address bus primitive for coupling to a first subset of the plurality of memory output primitives;

a second memory primitive;

a read data port primitive for coupling to the second memory primitive, the address bus primitive, and a second subset of the plurality of memory output primitives; and

a plurality of memory output primitives, each memory output primitive for coupling to the read data port primitive.

54. (New) The CAM-RAM model of Claim 53, wherein the compare port primitive includes:

a compare enable port;

a data bus port for coupling to an output port of the data bus primitive;

a data port for coupling to an output port of the memory primitive; and

an output port for coupling to input ports of the plurality of memory output primitives.

55. (New) A memory model compatible with a simulation tool and an automatic test pattern generation (ATPG) tool, the memory model including:

a plurality of primitives, each primitive representing a defined functionality of a memory.

56. (New) The memory model of Claim 55, wherein each primitive usable by the ATPG tool is configured based on a subset of behavioral hardware description language (HDL) usable by the simulation tool.

57. (New) The memory model of Claim 56, wherein the behavioral HDL includes Verilog.

58. (New) The memory model of Claim 56, wherein the subset of behavioral HDL can directly map to the plurality of primitives.